In the Claims

The following is a listing of the claims:

1. – 45. (Canceled)

46. (Currently Amended) A high f_{Max} deep submicron MOSFET structure, comprising:

a substrate;

a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode;

a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed and the first ILD layer is substantially flush with a top of the gate electrode;

a metal gate portion:

over the first ILD layer; and

over the silicide portion over the gate electrode;

the metal gate portion having a width substantially greater than the width of the silicide portion over the gate electrode;

a second ILD layer over the metal gate portion and the first ILD layer;

a first metal contact through the second ILD layer contacting the metal gate portion; and

a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{MAX} deep submicron MOSFET structure;

whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

47. (Original) The structure of claim 46, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

under the first ILD layer.

48. (Original) The structure of claim 46, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

between the first ILD layer;

the dielectric layer being comprised of Si_3N_4 or SiON.

49. (Original) The structure of claim 46, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of CoSix, $CoSi_2$, or $TiSi_2$; the first ILD layer is comprised of oxide, silicon oxide, USG or TEOS; the metal gate portion is comprised of W, Al, Cu, TiN or Au; the second ILD is comprised of oxide, silicon oxide, HDP or FSG; and the first and second metal contacts are each comprised of W or Cu.

50. (Original) The structure of claim 46, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of CoSix; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten; the second ILD is comprised of silicon oxide; and the first and second metal contacts each being comprised of tungsten.

51. (Original) The structure of claim 46, wherein the gate electrode has a width of from about 500 to 5000 Å and the metal gate portion has a width of from about 500 to 8000 Å.

52. (Original) The structure of claim 46, wherein the gate electrode has a width of from about 1000 to 3500 Å and the metal gate portion has a width of from about 1000 to 3000 Å.

53. (Original) The structure of claim 46, wherein the gate electrode has a width of about 0.13 μm and the metal gate portion has a width of from about 1800 to 2400 Å.

54. (Original) The structure of claim 46, wherein the gate electrode has a height of from about 1000 to 3000 Å; the silicide portion over the gate electrode has a thickness of from about 270 to 330 Å; the first ILD layer has a thickness of from about 1700 to 1900 Å; and the metal gate portion has a thickness of from about 1800 to 2200 Å.

55. (Original) The structure of claim 46, wherein the gate electrode has a height of from about 1500 to 2200 Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310 Å; the first ILD layer has a thickness of about 1800 Å; and the metal gate portion has a thickness of from about 1900 to 2100 Å.

56. (Original) The structure of claim 46, wherein the gate electrode has a height of from about 1500 to 2200 Å; the silicide portion over the gate electrode has a thickness of about 300 Å;

the first ILD layer has a thickness of about 1800 Å; and the metal gate portion has a thickness of about 2000 Å.

57. (Original) The structure of claim 46, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion the drain; and wherein the second metal contact contacts the drain silicide portion.

58. (Original) The structure of claim 46, wherein the MOSFET includes a source CoSix silicide portion over at least a portion of the source and a drain CoSix silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain CoSix silicide portion.

59. (Original) The structure of claim 46, wherein the first ILD is planarized.

60. (Original) The structure of claim 46, wherein the high f_{MAX} deep submicron MOSFET structure is positioned within an RF circuit.

61. (Original) The structure of claim 46, wherein the gate electrode has a gate oxide thereunder; the gate oxide having a thickness proximate the source and the drain to significantly reduce the parasitic capacitance and increase the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

62. (Currently Amended) A high f_{Max} deep submicron MOSFET structure, comprising:

a substrate;

a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode; the gate electrode having a width of from about 500 to 5000 Å;

a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed and the first ILD layer is substantially flush with a top of the gate electrode;

a metal gate portion:

over the first ILD layer; and

over the silicide portion over the gate electrode;

the metal gate portion having a width of from about 500 to 8000 Å;

a second ILD layer over the metal gate portion and the first ILD layer;

a first metal contact through the second ILD layer contacting the metal gate portion; and

a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{MAX} deep submicron MOSFET structure;

whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

63. (Original) The structure of claim 62, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

under the first ILD layer.

64. (Original) The structure of claim 62, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

between the first ILD layer;

the dielectric layer being comprised of Si_3N_4 or SiON.

65. (Original) The structure of claim 62, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of CoSix, $CoSi_2$, or $TiSi_2$; the first ILD layer is comprised of oxide, silicon oxide, USG or TEOS; the metal gate portion is comprised of W, Al, Cu, TiN or Au; the second ILD is comprised of oxide, silicon oxide, HDP or FSG; and the first and second metal contacts are each comprised of W or Cu.

66. (Original) The structure of claim 62, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of CoSix; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten; the second ILD is comprised of silicon oxide; and the first and second metal contacts each being comprised of tungsten.

67. (Original) The structure of claim 62, wherein the gate electrode has a width of from about 1000 to 3500 Å and the metal gate portion has a width of from about 1000 to 3000 Å.

68. (Original) The structure of claim 62, wherein the gate electrode has a width of about 0.13 μm and the metal gate portion has a width of from about 1800 to 2400 Å.

69. (Original) The structure of claim 62, wherein the gate electrode has a height of from about 1000 to 3000 Å; the silicide portion over the gate electrode has a thickness of from about 270 to 330 Å; the first ILD layer has a thickness of from about 1700 to 1900 Å; and the metal gate portion has a thickness of from about 1800 to 2200 Å.

70. (Original) The structure of claim 62, wherein the gate electrode has a height of from about 1500 to 2200 Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310 Å; the first ILD layer has a thickness of about 1800 Å; and the metal gate portion has a thickness of from about 1900 to 2100 Å.

71. (Previously amended) The structure of claim 62, wherein the gate electrode has a height of from about 1500 to 2200 Å; the silicide portion over the gate electrode has a thickness of about 300 Å; the first ILD layer has a thickness of about 1800 Å; and the metal gate portion has a thickness of about 2000 Å.

72. (Original) The structure of claim 62, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain silicide portion.

73. (Original) The structure of claim 62, wherein the MOSFET includes a source CoSix silicide portion over at least a portion of the source and a drain CoSix silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain CoSix silicide portion.

74. (Original) The structure of claim 62, wherein the high f_{MAX} deep submicron MOSFET structure is positioned within an RF circuit.

75. (Original) The structure of claim 62, wherein the gate electrode has a gate oxide thereunder; the gate oxide having a thickness proximate the source and the drain to significantly reduce the parasitic capacitance and increase the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

76. (Original) The structure of claim 62, wherein the first ILD is planarized.

77. (Currently Amended) A high f_{Max} deep submicron MOSFET structure, comprising:

a substrate;

a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode;

a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed and the first ILD layer is substantially flush with a top of the gate electrode;

a metal gate portion:

over the first ILD layer; and

over the silicide portion over the gate electrode;

the metal gate portion having a width substantially greater than the width of the silicide portion over the gate electrode;

whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

78. (Original) The structure of claim 77, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

under the first ILD layer.

79. (Original) The structure of claim 77, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

between the first ILD layer;

the dielectric layer being comprised of Si_3N_4 or SiON.

80. (Previously Presented) The structure of claim 77, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of CoSix, $CoSi_2$, or $TiSi_2$; the first ILD layer is comprised of oxide, silicon oxide, USG or TEOS; the metal gate portion is comprised of W, Al, Cu, TiN or Au.

81. (Previously Presented) The structure of claim 77, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of CoSix; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten.

82. (Original) The structure of claim 77, wherein the gate electrode has a width of from about 500 to 5000 Å and the metal gate portion has a width of from about 500 to 8000 Å.

83. (Original) The structure of claim 77, wherein the gate electrode has a width of from about 1000 to 3500 Å and the metal gate portion has a width of from about 1000 to 3000 Å.

84. (Original) The structure of claim 77, wherein the gate electrode has a width of about 0.13 μm and the metal gate portion has a width of from about 1800 to 2400 Å.

85. (Original) The structure of claim 77, wherein the gate electrode has a height of from about 1000 to 3000 Å; the silicide portion over the gate electrode has a thickness of from about 270 to 330 Å; the first ILD layer has a thickness of from about 1700 to 1900 Å; and the metal gate portion has a thickness of from about 1800 to 2200 Å.

86. (Original) The structure of claim 77, wherein the gate electrode has a height of from about 1500 to 2200 Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310 Å; the first ILD layer has a thickness of about 1800 Å; and the metal gate portion has a thickness of from about 1900 to 2100 Å.

87. (Original) The structure of claim 77, wherein the gate electrode has a height of from about 1500 to 2200 Å; the silicide portion over the gate electrode has a thickness of about 300 Å; the first ILD layer has a thickness of about 1800 Å; and the metal gate portion has a thickness of about 2000 Å.

88. (Previously presented) The structure of claim 77, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain.

89. (Previously Presented) The structure of claim 77, wherein the MOSFET includes a source CoSix silicide portion over at least a portion of the source and a drain CoSix silicide portion over at least a portion of the drain.

90. (Original) The structure of claim 77, wherein the first ILD is planarized.

91. (Original) The structure of claim 77, wherein the high f_{MAX} deep submicron MOSFET structure is positioned within an RF circuit.

92. (Previously Presented) The structure of claim 77, wherein the gate electrode has a gate oxide thereunder;

the gate oxide having a thickness proximate the source and the drain to significantly reduce the parasitic capacitance and increase the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

93. (Previously Presented) The structure of claim 77, further comprising:

a second ILD layer over the metal gate portion and the first ILD layer;

a first metal contact through the second ILD layer contacting the metal gate portion; and

a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{MAX} deep submicron MOSFET structure.

94. (Previously Presented) The structure of claim 93, wherein the first metal contact is a trench contact.

95. (Previously Presented) The structure of claim 93, wherein the second metal contact is a trench contact.